Semester:3rd	Department of Electronics and communication Engineering	AY: 2026-27
Course Code: 1BEC302	Course Name: Digital System Design Using Verilog	

Question Bank

Q.	Module-01	M	L	C
1.	Define combinational logic and state the differences between combinational and sequential circuits.	8	L2	CO1
2.	Design a combinational logic circuit that generates an output indicating when a majority of four inputs is true.	8	L2	CO1
3.	Develop the canonical minterm and maxterm forms for the Boolean equation: f(a,b,c) = a + b(a + c) + bc.	8	L2	CO1
4.	List the differences between a Prime Implicant (PI) and an Essential Prime Implicant (EPI).	6	L1	CO1
5.	Simplify the following Boolean function using the Quine-McCluskey (tabulation) method: f(a,b,c,d) = ∑ m(0, 1, 2, 6, 7, 9, 10, 12) with don't cares ∑ d(3, 5)	5	L3	CO1
6.	Design a logic circuit with 3 input variables that produces a high output when more than two inputs are high.	6	L3	CO1
7.	Simplify a 4-variable Boolean expression using Karnaugh Maps (K-map) and handle specified don't-care conditions.	5	L3	CO1
8.	Analyze an industrial control scenario: Design an electric motor/conveyor interlock logic based on operator position, material presence, and safety switch status.	8	L4	CO1
9.	Convert a given standard sum-of-products (SOP) expression into a product-of-sums (POS) canonical form.	5	L3	CO1
10.	Implement a given 4-variable logic function using basic logic gates starting from a truth table.	6	L3	CO1
	Module-02			
11.	Explain the operation of a full adder and derive its sum and carry logic expressions.	9	L2	CO2
12.	Describe the internal architecture and propagation delay of a 4-bit Carry Look-Ahead (CLA) adder.	8	L2	CO2
13.	Design a 2-bit binary magnitude comparator using a cascade connection of 1-bit comparators.	8	L3	CO2
14.	Construct the truth table, logic equations, and circuit diagram for a 3:8 line decoder.	8	L3	CO2
15.	Explain the working of an 8:3 priority encoder with a truth table and Boolean expressions.	7	L2	CO2
16.	Design an 8:1 multiplexer and show how to implement a larger boolean function using it.	8	L3	CO2

Aditya College of Engineering and Technology

17.	Construct a parallel binary adder/subtractor circuit using full adders and XOR gates.	8	L3	CO2
18.	Explain BCD (decimal) adders with a block diagram and derive the binary-to-BCD correction logic.	9	L2	CO2
19.	Realize a given multi-output Boolean function using a combination of a decoder and external logic gates.	7	L3	CO2
20.	Discuss the architectural differences between a PROM, a PLA, and a PAL.	7	L2	CO2
	Module-03			
21.	Explain the major data types available in Verilog HDL (nets, reg, integer, parameter) with code examples.	8	L2	CO3
22.	Evaluate bitwise, arithmetic, and logical Verilog operators given sample vector values (e.g., A = 4'b0011, B = 4'b0100).	5	L3	CO3
23.	Write a Verilog dataflow model for a full subtractor.	6	L3	CO3
24.	Explain the three primary styles of description in Verilog (Gate-level/Structural, Dataflow, and Behavioral) using a half adder as an example.	8	L2	CO3
25.	Write a Verilog structural description program for an 8:1 multiplexer including a block diagram reference.	8	L3	CO3
26.	Write a Verilog structural code for a 4-bit ripple carry adder.	7	L3	CO3
27.	Explain module declaration, port lists (input, output, inout), and instantiation rules in Verilog.	7	L2	CO3
28.	Write a Verilog dataflow description of a 4-bit magnitude comparator using continuous assignment (assign).	7	L3	CO3
29.	Differentiate between blocking (=) and non-blocking (<=) procedural assignments with code snippets.	7	L4	CO3
30.	Write a Verilog behavioral description for a 3-bit binary up-counter	6	L3	CO3
	Module-04			
31.	Construct the logic diagram and truth table of a Master-Slave JK flip-flop along with its timing diagram.	8	L3	CO4
32.	Derive the characteristic equation and excitation table for SR, JK, D, and T flip-flops.	10	L3	CO4
33.	Explain switch debouncing using an SR latch circuit.	6	L2	CO4
34.	Construct a Johnson counter using positive edge-triggered D flip-flops and explain its state sequence.	8	L3	CO4
35.	Explain the architecture and mode-control table of a universal shift register.	8	L2	CO4
36.	Design a synchronous counter that follows the sequence 0 → 2 → 5 → 0 using T flip-flops.	9	L3	CO4
37.	Design an asynchronous (ripple) 3-bit binary up/down counter and draw its waveform.	8	L3	CO4

Aditya College of Engineering and Technology

38.	Explain the design and working of a ring counter and a twisted-ring (Johnson) counter.	8	L2	CO4
39.	Analyze mod-N counter design techniques using JK and D flip-flops (e.g., Mod-6 or Mod-12).	8	L4	CO4
40.	Differentiate between synchronous and asynchronous counters in terms of clocking, speed, and glitch hazards.	7	L4	CO4
	Module-05			
41.	Realize a D-latch using Verilog behavioral description along with its circuit diagram and waveform.	8	L3	CO5
42.	Explain the syntax and execution behavior of Verilog sequential loop statements: for, while, repeat, and forever.	8	L2	CO5
43.	Write a Verilog program for an 8:1 multiplexer using the case statement.	7	L3	CO5
44.	Realize a JK flip-flop using Verilog behavioral description (always @(posedge clk)).	7	L3	CO5
45.	Explain the operation of a half adder and implement it using structural description in Verilog.	7	L3	CO5
46.	Explain the syntax and structure of the Verilog case statement (including case, casex, and casez).	7	L2	CO5
47.	Develop a Verilog behavioral description code for a D-latch.	6	L3	CO5
48.	Write a Verilog behavioral model for a JK flip-flop with asynchronous reset/preset control.	8	L3	CO5
49.	Write a basic Verilog testbench module (initial block, $display, $monitor, and stimulus generation) to verify a combinational circuit.	8	L3	CO5
50.	Explain the significance of sensitivity lists (always @(...)) in behavioral simulation and how edge-triggered events differ from level-sensitive events.	8	L2	CO5

***Note:**

1. All modules should contain a minimum of **10** questions each and the total number of questions must be **50**.
2. Questions can carry marks of 06, 07, 08, 09, 10 and for problems: 04 or 05.
3. Follow the RBTL as per the keywords used to frame the questions.
4. Maintain the Course Outcomes (COs) as per the syllabus.
5. M: Marks, L: RBTL, C:COs.

Aditya College of Engineering and Technology