Semester: V	Department of Electronics and computer system	AY: 2026-27
Course Code: BUE515B	Course Name: Advanced computer architecture	

Question Bank

Q.	Module-01	M	L	C
1.	Explain parallel computer models and compare shared-memory and distributed-memory models.	7	L2	CO1
2.	Write a brief note on - Physical significance of wave function, Principle of complementarily, Expectation value& Quantum tunneling.	7	L2	CO1
3.	Differentiate SIMD and MIMD computers with suitable examples.	6	L2	CO1
4.	Explain PRAM models and VLSI models used in parallel computation.	8	L2	CO1
5.	Discuss program and network properties that influence parallel processing.	6	L2	CO1
6.	Explain the conditions of parallelism and identify dependencies that limit parallel execution.	7	L2	CO1
7.	Describe program partitioning and scheduling in a parallel system.	6	L2	CO1
8.	Explain program flow mechanisms and system interconnect architectures.	8	L2	CO1
9.	Discuss the principles of scalable performance and explain performance metrics and measures.	7	L2	CO1
10.	State and explain speedup performance laws. Illustrate one law with a numerical example.	7	L2	CO1
	Module-02			
11.	Explain processor and memory hierarchy in a computer system.	6	L2	CO2
12.	Describe advanced processor technology and its major design features.	7	L2	CO2
13.	Explain the organization and operation of a superscalar processor.	6	L2	CO2
14.	Describe vector processors and explain how vector operations improve performance.	7	L2	CO2
15.	Compare scalar, superscalar and vector processor architectures.	5	L2	CO2
16.	Explain memory hierarchy technology and the need for multiple levels of memory.	6	L2	CO2
17.	Discuss cache memory, main memory and secondary storage in the memory hierarchy.	8	L2	CO2
18.	Explain virtual memory technology and address translation.	7	L2	CO2
19.	Describe the role of page tables and TLBs in virtual memory.	6	L2	CO2
20.	Compare physical memory and virtual memory, stating their advantages.	6	L2	CO2

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Module-03				
21.	Explain bus systems and discuss the different bus organizations.	7	L2	CO3
22.	Describe cache memory organization with a neat block diagram.	6	L2	CO3
23.	Explain shared-memory organizations and their characteristics.	6	L2	CO3
24.	Differentiate sequential consistency and weak consistency models.	7	L2	CO3
25.	Explain pipelining and discuss the stages of a linear instruction pipeline.	7	L2	CO3
26.	Describe the operation of a superscalar processor and its pipeline structure.	6	L2	CO3
27.	Explain the working of a linear pipeline processor with an example.	7	L2	CO3
28.	What are pipeline hazards? Explain structural, data and control hazards.	8	L2	CO3
29.	Describe nonlinear pipeline processors and compare them with linear pipelines.	8	L2	CO3
30.	Explain how pipeline performance is evaluated using throughput and speedup.	7	L2	CO3
Module-04				
31.	Compare multiprocessors and multicomputers with suitable examples.	6	L2	CO4
32.	Explain multiprocessor system interconnects and compare common interconnection networks.	7	L2	CO4
33.	Describe cache coherence and explain the need for cache synchronization mechanisms.	6	L2	CO4
34.	Explain message-passing mechanisms in parallel architectures.	7	L2	CO4
35.	Discuss multivector and SIMD computers and their applications.	7	L2	CO4
36.	Explain vector processing principles and multivector multiprocessors.	8	L2	CO4
37.	Describe compound vector processing and its advantages.	7	L2	CO4
38.	Explain scalable, multithreaded and dataflow architectures.	8	L2	CO4
39.	Discuss latency-hiding techniques used in parallel systems.	6	L2	CO4
40.	Explain the principles of multithreading and fine-grain multicomputers.	7	L2	CO4
Module-05				
41.	Explain parallel models, languages and compilers used for parallel programming.	8	L2	CO5
42.	Discuss parallel programming models and compare shared-memory and message-passing approaches.	7	L2	CO5
43.	Explain parallel languages and compilers and their role in parallel software development.	6	L2	CO5
44.	Describe dependence analysis of data arrays and its importance in parallelization.	7	L2	CO5
45.	Differentiate instruction-level parallelism and system-level parallelism.	7	L2	CO5

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46.	Explain the basic design issues in instruction-level parallelism.	6	L2	CO5
47.	Describe the model of a typical processor and identify features that support parallel execution.	8	L2	CO5
48.	Explain compiler-detected instruction-level parallelism and operand forwarding.	7	L2	CO5
49.	Discuss reorder buffers and register renaming with suitable examples.	6	L2	CO5
50.	Explain Tomasulo's algorithm and show how it supports dynamic scheduling.	7	L2	CO5

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