Semester:5th	Department of Electronics and communication Engineering	AY: 2026-27
Course Code: BUE503	Course Name: Digital System Design Using Verilog	

Question Bank

Q.	Module-01	M	L	C
1.	Define design methodology. Explain the top-down and bottom-up design approaches with a neat block diagram.	8	L2	CO1
2.	List and explain the IC technology options (full-custom, semi-custom, gate array, PLD, FPGA) available for implementing digital designs.	8	L2	CO1
3.	What are glitches and hazards in combinational logic? Explain static-1, static-0 and dynamic hazards with examples.	8	L2	CO1
4.	Detect the static hazard in f(a,b,c) = ab + b'c using a K-map and show how it is eliminated.	5	L2	CO1
5.	Define the following terms: (a) Structural model (b) Logic system (c) Propagation delay (d) Design verification.	6	L1	CO1
6.	Explain the structural model of combinational logic in Verilog using gate primitives, with a 2:1 multiplexer as an example.	8	L2	CO1
7.	Explain the four-valued logic system and the signal strength levels used in Verilog.	7	L2	CO1
8.	Describe the design verification and test methodology with a block diagram of a testbench.	8	L2	CO1
9.	Explain propagation delay (rise, fall and turn-off) and how it is modelled in Verilog gate primitives using min:typ:max delays.	7	L2	CO1
10.	Explain truth-table models of combinational and sequential logic using Verilog user-defined primitives (UDPs) with examples.	9	L2	CO1
	Module-02			
11.	Explain behavioural modelling in Verilog and discuss the data types (reg, integer, real, time) used in behavioural models.	7	L2	CO2
12.	Write a Boolean-equation-based behavioural model of a full adder using continuous assignments.	6	L3	CO2
13.	Explain propagation delay and continuous assignments in Verilog with examples (regular and implicit assignment delays).	7	L2	CO2
14.	Explain latches and level-sensitive circuits in Verilog. How are unintended latches inferred and how can they be avoided?	7	L2	CO2
15.	Write Verilog cyclic behavioural models of a D flip-flop with asynchronous reset and a D latch.	8	L3	CO2
16.	Explain cyclic behaviour and edge detection in Verilog using the always statement with posedge and negedge.	7	L2	CO2
17.	Explain the different styles of behavioural modelling (dataflow,	8	L2	CO2

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	cyclic behaviour, algorithmic) using a 2:1 multiplexer as an example.			
18.	Write behavioural Verilog models of a 4:1 multiplexer, a 2:4 decoder and a 4:2 priority encoder.	10	L3	CO2
19.	Write a dataflow Verilog model of a 4-bit Linear-Feedback Shift Register (LFSR) and explain its operation.	8	L3	CO2
20.	Explain functions and tasks in Verilog for design documentation, with examples. Discuss when each should be used.	8	L2	CO2
	Module-03			
21.	What is an Algorithmic State Machine (ASM) chart? Explain its basic elements (state box, decision box, conditional output box) with an example.	8	L2	CO3
22.	Draw the ASM chart for a Mealy sequence detector that detects the sequence 1011 and write its behavioural Verilog description.	10	L3	CO3
23.	Explain the relationship between an ASM chart and a state-transition graph with a suitable example.	6	L2	CO3
24.	Write a behavioural Verilog model of a 4-bit synchronous up/down counter with parallel load and asynchronous reset.	8	L3	CO3
25.	Develop a behavioural Verilog model of a 4-bit shift register with parallel load and serial-in/serial-out, and explain its operation.	8	L3	CO3
26.	Write a behavioural Verilog model of a register file with one write port and two read ports.	8	L3	CO3
27.	What is synthesis? Explain the steps in the synthesis flow (RTL description, logic synthesis, optimization, technology mapping).	7	L2	CO3
28.	Explain the synthesis of combinational logic from Verilog descriptions (assign, if, case) and the problems caused by incomplete assignments.	7	L2	CO3
29.	Explain how latches are inferred in the synthesis of sequential logic from Verilog, with examples.	7	L2	CO3
30.	List the guidelines for writing synthesizable Verilog descriptions of combinational and sequential logic.	6	L1	CO3
	Module-04			
31.	Explain the design procedure for sequential machines. Distinguish Moore and Mealy models with block diagrams.	8	L2	CO4
32.	Draw the state-transition graph and state table of a Moore machine that detects the sequence 101.	8	L3	CO4
33.	Design a BCD to Excess-3 code converter as a sequential machine: derive the state-transition graph, state table and Verilog description.	10	L3	CO4

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34.	Design a serial-line code converter for data transmission (NRZ to NRZI) using a state-transition graph and write its Verilog model.	10	L3	CO4
35.	Explain the synthesis of explicit state machines with a Verilog example.	8	L2	CO4
36.	Explain the synthesis of implicit state machines with an example and state how it differs from explicit state machines.	8	L2	CO4
37.	Write a synthesizable Verilog model of a 4-bit register with synchronous load and asynchronous reset.	7	L3	CO4
38.	Design and write a Verilog model of a mod-10 (BCD) counter and explain how counters are synthesized.	8	L3	CO4
39.	List the differences between Moore and Mealy machines with examples.	6	L1	CO4
40.	Explain the state-encoding techniques (binary, Gray and one-hot) used in the synthesis of state machines.	7	L2	CO4
	Module-05			
41.	Explain the classification of programmable logic devices (SPLD, CPLD, FPGA) with block diagrams.	8	L2	CO5
42.	Explain the different storage devices: ROM, PROM, EPROM, EEPROM and Flash memory.	8	L2	CO5
43.	Explain the architecture of a Programmable Logic Array (PLA) with a neat diagram.	8	L2	CO5
44.	Explain the architecture of a Programmable Array Logic (PAL) with a neat diagram.	8	L2	CO5
45.	List the differences between a PLA and a PAL.	6	L1	CO5
46.	Explain the programmability technologies of PLDs (fuse, antifuse, EPROM, EEPROM and SRAM based).	8	L2	CO5
47.	Describe the architecture of a Complex PLD (CPLD) with a block diagram of function blocks, macrocells and interconnect.	9	L2	CO5
48.	Describe the architecture of an FPGA, explaining the CLB, I/O block and routing resources.	9	L2	CO5
49.	List the advantages of programmable logic devices over fixed-function ICs.	6	L1	CO5
50.	Explain the FPGA design flow (design entry, synthesis, place and route, bitstream generation).	8	L2	CO5

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***Note:**

1. All modules should contain a minimum of **10** questions each and the total number of questions must be **50**.
2. Questions can carry marks of 06, 07, 08, 09, 10 and for problems: 04 or 05.

3. Follow the RBTL as per the keywords used to frame the questions.
4. Maintain the Course Outcomes (COs) as per the syllabus.
5. M: Marks, L: RBTL, C:COs.

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