Semester: 7	Department of Electronics & Computer Engineering	AY: 2026-27
Course Code: BUE702	Course Name: SystemVerilog	

Question Bank

Q.	Module-01	M	L	C
1.	Explain the verification process in SystemVerilog.	10	L2	CO1
2.	Draw the diagram of the layered testbench of SystemVerilog and describe the function of each layer.	10	L2	CO1
3.	Explain the factors in randomizing the stimulus to a design.	10	L2	CO1
4.	Describe fixed-size arrays in SystemVerilog with examples.	6	L2	CO1
5.	Describe dynamic arrays in SystemVerilog with examples.	6	L2	CO1
6.	Describe the various array methods in SystemVerilog with examples.	8	L2	CO1
7.	Write a note on user-defined data types (typedef) in SystemVerilog with examples.	6	L2	CO1
8.	Describe enumerated data types in SystemVerilog with examples.	6	L2	CO1
9.	Explain constants in SystemVerilog with examples.	6	L2	CO1
10.	Explain strings and string methods in SystemVerilog with examples.	6	L2	CO1
	Module-02			
11.	Describe C-style routine arguments and argument direction in SystemVerilog with program examples.	6	L2	CO2
12.	Describe advanced argument types and default argument values in SystemVerilog with program examples.	6	L2	CO2
13.	Explain tasks, functions and void functions in SystemVerilog.	6	L2	CO2
14.	Write the differences between tasks and functions in SystemVerilog.	6	L2	CO2
15.	Explain automatic storage and variable initialization with a SystemVerilog program example.	8	L3	CO2
16.	How are time values specified in SystemVerilog? Describe with examples.	7	L2	CO2
17.	Draw the diagram of the testbench–arbiter without interface and write the SystemVerilog code for the arbiter model using ports, the testbench using ports and the top-level netlist without interface.	10	L3	CO2
18.	Describe the communication between the testbench and the DUT with a suitable diagram and SystemVerilog program.	10	L3	CO2
19.	Describe the testbench–design race condition. Write SystemVerilog code for a race condition between the testbench and the design.	8	L3	CO2
20.	Explain the different types of SystemVerilog assertions with examples.	10	L2	CO2
	Module-03			

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21.	What is randomization? Explain the concept of randomization in SystemVerilog with an example.	10	L2	CO3
22.	Describe solution probabilities in SystemVerilog with examples.	10	L2	CO3
23.	Explain valid constraints in SystemVerilog with examples.	6	L2	CO3
24.	Explain in-line constraints in SystemVerilog with examples.	6	L2	CO3
25.	Describe conditional constraints in SystemVerilog with examples.	6	L2	CO3
26.	Describe bidirectional constraints in SystemVerilog with examples.	6	L2	CO3
27.	Discuss the common randomization problems in SystemVerilog with a program.	6	L3	CO3
28.	Describe the operation of the randcase statement with a program.	6	L3	CO3
29.	Write any four random number functions in SystemVerilog with examples.	8	L3	CO3
30.	Write a note on pseudo-random number generators in SystemVerilog.	6	L2	CO3
	Module-04			
31.	What are SystemVerilog threads? Explain fork…join, fork…join_none and fork…join_any statements with examples.	10	L2	CO4
32.	Write SystemVerilog code for creating threads in a class with a task that creates packets.	8	L3	CO4
33.	Describe the concept of dynamic thread creation with SystemVerilog code.	6	L3	CO4
34.	Describe how a single thread and multiple threads are disabled in SystemVerilog.	6	L2	CO4
35.	What is an event? Write a program for passing an event into a constructor.	6	L3	CO4
36.	Explain waiting for an event trigger and using events in a loop.	10	L2	CO4
37.	What is a semaphore in SystemVerilog? Explain the semaphore operations.	6	L2	CO4
38.	Describe the semaphore operations by writing a SystemVerilog program.	6	L3	CO4
39.	What is a mailbox in SystemVerilog? Explain the exchange of objects using a mailbox with a suitable example.	10	L3	CO4
40.	Explain the use of events, semaphores and mailboxes for interprocess communication in SystemVerilog.	10	L2	CO4
	Module-05			
41.	What is coverage? Describe the different coverage types in SystemVerilog.	10	L2	CO5
42.	Describe the various functional coverage strategies.	10	L2	CO5
43.	Explain functional coverage inside a class with a program.	7	L3	CO5
44.	Write a note on data sampling in functional coverage.	6	L2	CO5

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45.	Explain how cover points and bins (automatic and user-defined) are defined, with an example.	8	L3	CO5
46.	What is cross coverage? Write the code for basic cross coverage and give the coverage summary report.	10	L3	CO5
47.	Write the code for labelling cross coverage bins and give its summary report.	10	L3	CO5
48.	Explain generic cover groups in SystemVerilog.	10	L2	CO5
49.	Describe the various coverage options with examples.	10	L2	CO5
50.	Explain how coverage data is measured and analysed in a SystemVerilog verification environment.	8	L2	CO5

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